Low Static Power and High Bit Rate Wave-Pipelined Global Interconnect Circuits

Undergraduate Thesis Proposal by Mark Youngblood

I. Introduction

As every successive generation of Very Large Scale Integrated (VLSI) systems house a higher number of transistors, the power dissipation that takes place during inactive circuit periods (when power is running through the wires but transistor switching is not taking place) has become one of the greatest limitations to improvements in system performance. This static power dissipation takes place primarily through the transistor interconnects, or wiring that connects each transistor into the circuit network. With the shrinking size of application specific integrated circuits (ASICs) and increased number of transistors per chip, the complexity and number of semi-global and global interconnects will continue to increase [1]. Due to a higher number of interconnects and an associated increase in the static power dissipation, developing low-power interconnect circuit techniques is imperative for future systems.

Using HSPICE simulations of future transistor technologies ranging from a gate size of 90nm to 22nm, this proposed research will demonstrate that increasing threshold voltages (the boundary between a “one” or “zero” in a transistor) can substantially reduce static power dissipation throughout the interconnects. As an unintentional side-effect, this increase in threshold voltage will reduce the speed of the circuit; however, it is the hypothesis of this proposed research that the wave-pipelining throughput can be boosted by the insertion of buffers (or repeaters) to
compensate for this performance loss. The insertion of buffers will allow the circuit to operate in stages, so that multiple signals can be sent simultaneously and the throughput of the circuit will be increased. It is expected that the latency will suffer with high-threshold voltage repeaters design, but it is assumed that the benefits in throughput and power dissipation will outweigh this potential drawback. A major product of this research will be to find an optimal combination of threshold voltages and number of repeaters to minimize static power loss and maximize throughput.

This research project will explore a low-power, high-throughput design using high threshold voltage buffers in combination with wave-pipelining techniques to produce VLSI interconnect networks with high throughput performance and low static (inactive) power dissipation.

Reducing the static power consumption of integrated circuits will lead to more power efficient devices. Through the use of wave-pipelining, an increase in throughput will create faster, higher frequency operating circuits. This proposal will describe the process to carry out research on this topic. Section 2 considers current work in this area. Section 3 will give a formal definition of the research problem and the proposed methods for solving it. Section 4 provides a detailed, bi-monthly work-schedule.

II. Current Work

The International Technology Roadmap for Semiconductors (ITRS) [2] has detailed impending power dissipation rates as transistor gates approach the 22 nm size. In general, work has investigated several aspects of decreased dynamic power dissipation (power dissipated when a transistor is switching) and increased throughput
of wave-pipelined interconnect circuits, but there has been very little work in optimizing wave-pipelined interconnect networks for low static power dissipation.

**Wave-Pipelining and Voltage Scaling**

Work conducted by Deodhar in [3] explores the reduction of dynamic power dissipation in high-density VLSI circuits through the reduction of supply voltages. With dynamic power as a function of the square of the supply voltage, a reduction in this variable will lead to considerable reductions in dynamic power [3]. However as a consequence of lower supply voltages, transistors will experience smaller drive current thereby reducing circuit performance. The authors in [3] propose to compensate for this loss in interconnect circuit performance through the use of additional repeater insertion.

In addition, the authors in [3] develop an optimization between the supply voltage and number of repeaters to generate minimum dynamic power loss with maximum throughput. Using throughput per bit-energy as a metric, they conclude that the optimum supply voltage is 1V with 30 repeaters. This arrangement gives a latency (i.e. delay) approximately equal to that with no repeaters but a throughput that has increased by an order of magnitude.

**Static Power Dissipation**

Reduction in static power dissipation has been suggested by H. Heogun, R. Senger, D. Sylvester, R. Brown, and K. Nowka through the use of a dual-VDD bus technique [4]. The new technique improves the traditional static pulsed bus design [5] which operates by supplying the bus invertors with a VDD high enough to ensure correct operation only during transition periods. The supply voltage is reduced during
quiescent periods so that power is not wasted. With power supply varying based on
the state of the circuit (quiescent with low VDD vs. transitioning with high VDD), the
static power dissipation can be drastically reduced during quiescent periods.

Improvement is made by only modulating VDD on even inverter stages of the
bus. According to [4], ‘The power supply boost occurs only for the even half of the
bus line repeaters since the odd stages drive an inverted pulse from VDD_L to 0 V to
VDD_L and thus do not need the VDD_H boost’. Typically VDD_L (the lower
supply voltage) is 0.7 * VDD_H [6, 7]. Improvement using this method compared to
a traditional static bus and static pulsed bus is shown in Table I after [4].

<table>
<thead>
<tr>
<th>Bus Design Technique</th>
<th>Dynamic Power</th>
<th>Static Power</th>
<th>Delay</th>
<th>Dynamic/Static Power Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Traditional Static Bus</td>
<td>1.00</td>
<td>1.00</td>
<td>1.00</td>
<td>11.1 / 1</td>
</tr>
<tr>
<td>Static Pulsed Bus</td>
<td>0.76</td>
<td>0.78</td>
<td>0.97</td>
<td>10.9 / 1</td>
</tr>
<tr>
<td>Dual-V_{dd} Boosted Pulse Bus</td>
<td>0.51</td>
<td>0.28</td>
<td>0.85</td>
<td>20.4 / 1</td>
</tr>
</tbody>
</table>

### III. Research Problem

The intention of this project is to demonstrate that a low static power, high
throughput interconnect repeater circuit can be constructed through the use of low
threshold voltages and wave-pipelining. The research problem to be investigated hinges
on a problem defined by the International Roadmap for Semiconductors; namely that
the management of overall power consumption (particularly static power) is one of the major challenges facing the semiconductor industry.

Over past semesters, work has been performed to verify that the simulation models in [8] that will be used in this work do indeed predict that static power dissipation will significantly increase over the next 10 years. These transistor HSPICE models in [8] will be used with interconnect models to simulate the power dissipation in a variety wave-pipelined interconnect circuit configurations. In particular, work so far has demonstrated that static power dissipation for a basic inverter will increase substantially with every technology generation. The test circuit used to measure the static power consumption data appears in Figure 1.

![CMOS inverter circuit configuration used for static power extraction](image)

Figure 1: CMOS inverter circuit configuration used for static power extraction

Power dissipation measurements were taken using HSPICE software for various technology nodes. These results are listed in Table II. The static power as a percentage of total power was also calculated and appears in this table. In order to perform the simulations at different technology nodes, the gate widths and supply voltage were scaled down by the same factor as the gate length in accordance with the ITRS. As seen in Figure 2, the percentage of power that is static power increases exponentially. These
results demonstrate that as circuit technology continues to progress (get smaller), static power is becoming a larger percentage of the total power consumption and if left unchecked will dominate overall power consumption as transistor gates pass the 22nm length. With this data in mind, the proposed project will offer a technique to reduce the static power consumption and alleviate this growing problem.

Table II: HSPICE simulation results of static power until 22nm node

<table>
<thead>
<tr>
<th>Length (nm)</th>
<th>Width (um)</th>
<th>$V_{dd}$</th>
<th>Static Power</th>
<th>Static %</th>
</tr>
</thead>
<tbody>
<tr>
<td>130</td>
<td>25.26</td>
<td>1.3</td>
<td>9.12E-07</td>
<td>2.767</td>
</tr>
<tr>
<td>90</td>
<td>17.4888</td>
<td>1.2</td>
<td>9.35E-07</td>
<td>4.99</td>
</tr>
<tr>
<td>65</td>
<td>12.6308</td>
<td>1.1</td>
<td>8.93E-07</td>
<td>6.88</td>
</tr>
<tr>
<td>45</td>
<td>8.7444</td>
<td>1.0</td>
<td>8.21E-07</td>
<td>9.96</td>
</tr>
<tr>
<td>32</td>
<td>6.21824</td>
<td>0.9</td>
<td>1.10E-06</td>
<td>16.9</td>
</tr>
<tr>
<td>22</td>
<td>4.27504</td>
<td>0.7</td>
<td>1.90E-06</td>
<td>22.5</td>
</tr>
</tbody>
</table>
The remaining work in this research project involves designing global interconnect circuits and running simulations to verify the stated hypothesis. Using the circuit in Figure 1 as a basic building block, on-chip global interconnects, which will be modeled as distributed RLC transmission lines, will be inserted and the threshold voltages modulated to different levels to measure changes in both static power consumption and channel throughput. For a given interconnect circuit, we expect that higher threshold voltages will lead to exponential decreases in static power dissipation, but only a linear decrease in the throughput. Additional high-$V_T$ repeaters will be inserted into the global interconnects in an effort to increase throughput while keeping low static power loss.
IV. Work Plan and Schedule

<table>
<thead>
<tr>
<th>Period</th>
<th>Goal(s)</th>
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| July 22-31         | • Finish thesis proposal  
|                    | • Conclude dynamic power simulations for 22nm, 32nm, 45nm, 65nm, & 180nm technologies                                                   |
| August 1 – 31      | • Run static and dynamic power simulations with inclusion of interconnects                                                                |
| September 1 – 30   | • Using HSPICE measure interconnect bitrate  
|                    | • Change number of repeaters in circuits and note changes on throughput and power dissipation                                             |
| October 1 – 13     | • Determine optimization methodology using analytical expressions                                                                         |
| October 14 – 31    | • Determine optimal number of repeaters and threshold voltages in circuit using simulations                                                  |
| November 1 – 30    | • Write thesis paper                                                                                                                       |
| December 1 - 7     | • Thesis presentation                                                                                                                      |

The possible research targets that could be met in the final dissertation are as follows:

**Low Target**

The thesis will illustrate at least a few examples of non-optimized interconnect repeater circuits with high-$V_T$ and low-$V_T$ devices along the ITRS roadmap.

**Expected Target**

In addition to the low target results, the thesis is expected to illustrate a design methodology of optimal interconnect repeater circuits with low-static power under the constraint of throughput values given by ITRS projections.

**High Target**

Finally, a high target for this thesis would be to also include ideal power supply voltage scaling along with optimal threshold voltages. This optimization would minimize both dynamic and static power dissipation simultaneously.
References


