Target ASIC Design Flow

Flow | Files | Verification | Simulation
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Behavioral HDL | Behavioral HDL | NC-Verilog | NC-Verilog
SOC-Encounter Synopsys | SOC-Encounter Synopsys | NC-VHDL | NC-VHDL
Behavioral | Behavioral | NC-Sim | NC-Sim
RTL | RTL | MMSIM IUS | MMSIM IUS
High level synthesis | Technology Mapping | SOC Synopsys | SOC Synopsys
Gate level netlist | Gate level netlist | Conformal LEC | Conformal LEC
Cadence | Cadence | Switch Level | Switch Level
Conformal LEC | Conformal LEC | Timing | Timing
Schematic | Schematic | Assura LVS | Assura LVS
Place & Route | Layout | Assura DRC | Assura DRC
SOC-Encounter | SOC-Encounter | Cadence | Cadence
Conformal LEC | Conformal LEC | NC-Verilog | NC-Verilog
Hspice | Hspice | Spectre | Spectre
Fast spice | Fast spice | UltraSim | UltraSim
Critical paths | Critical paths | Hspice Spectre | Hspice Spectre

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